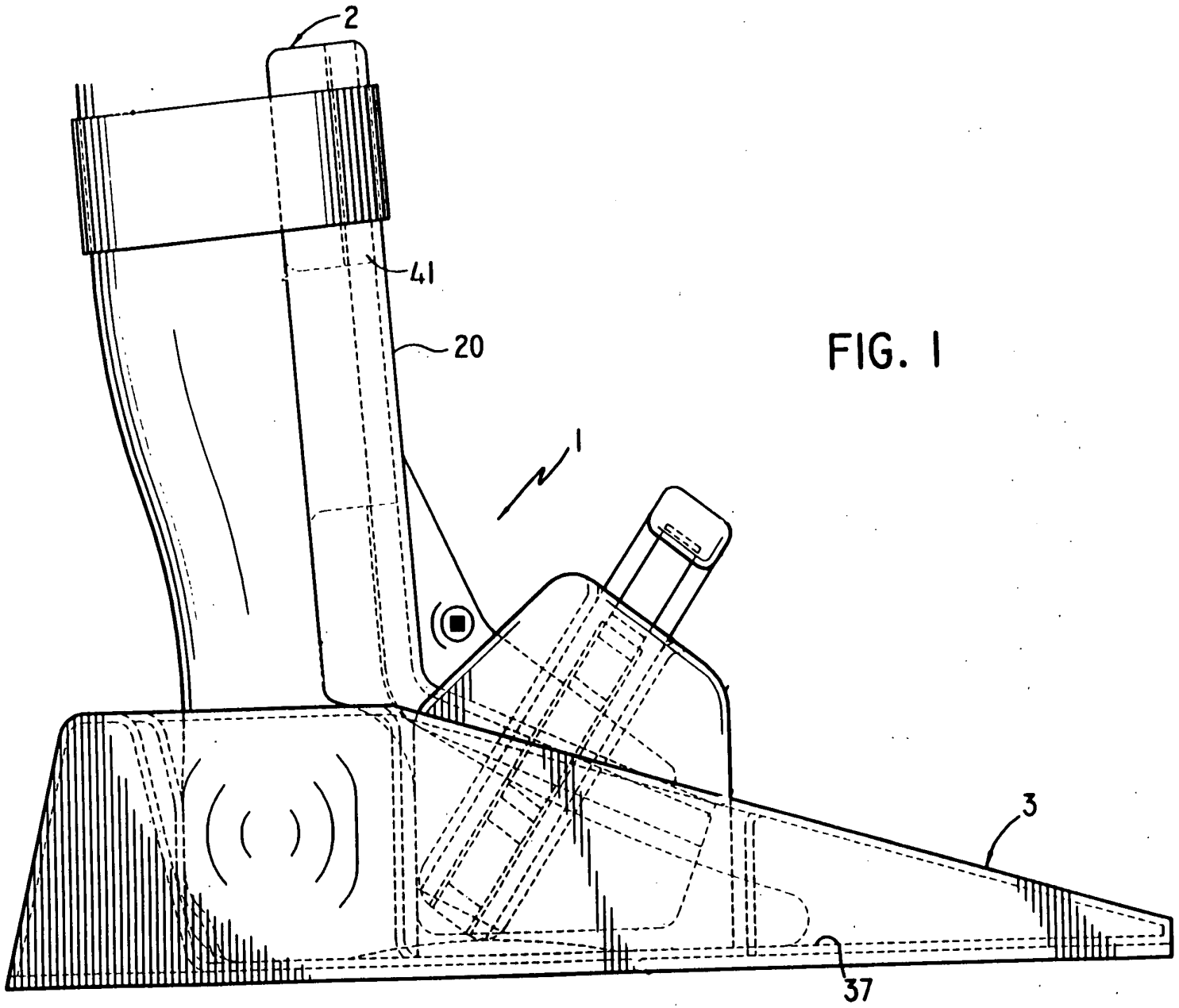


FIG. 1

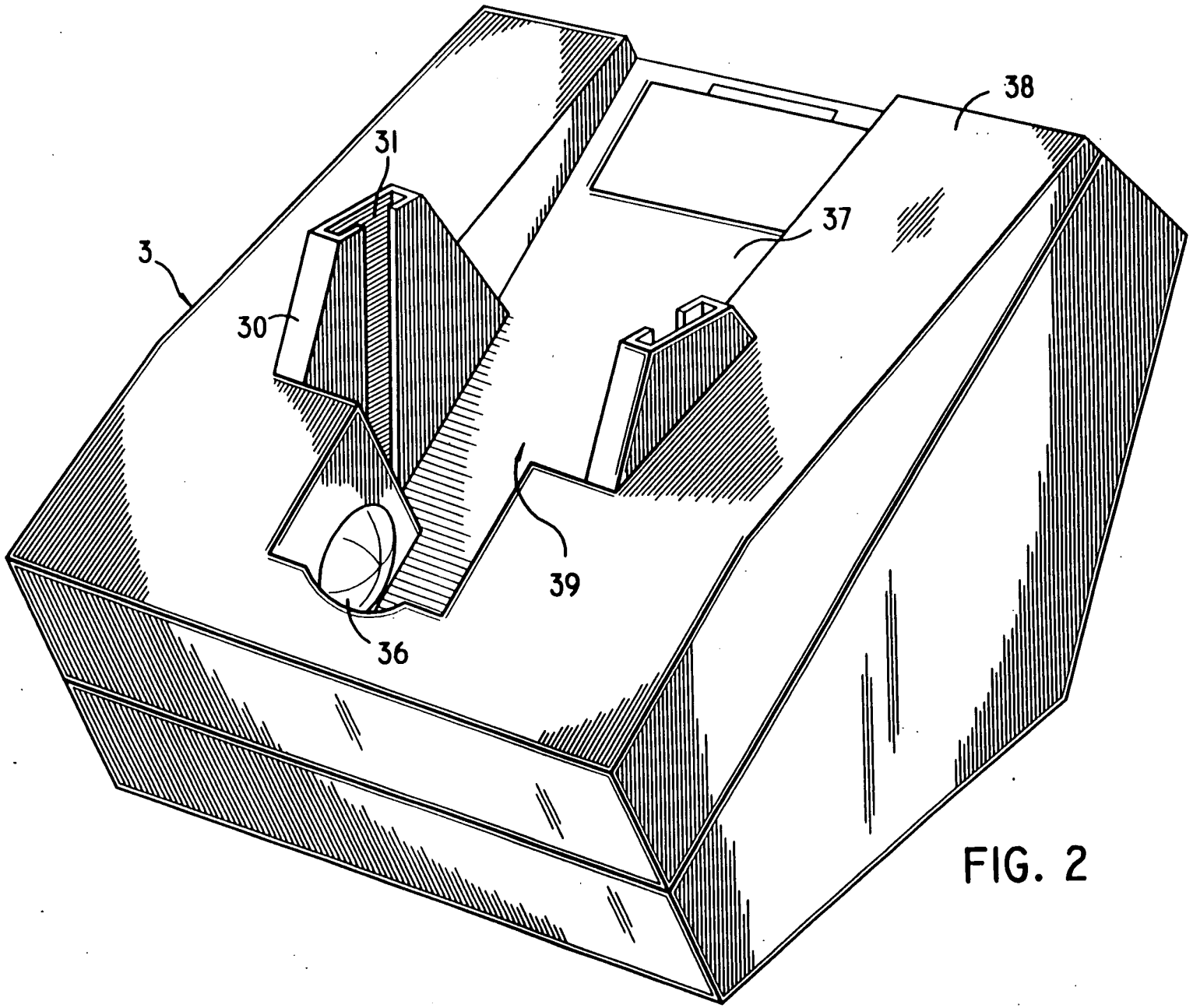


FIG. 2

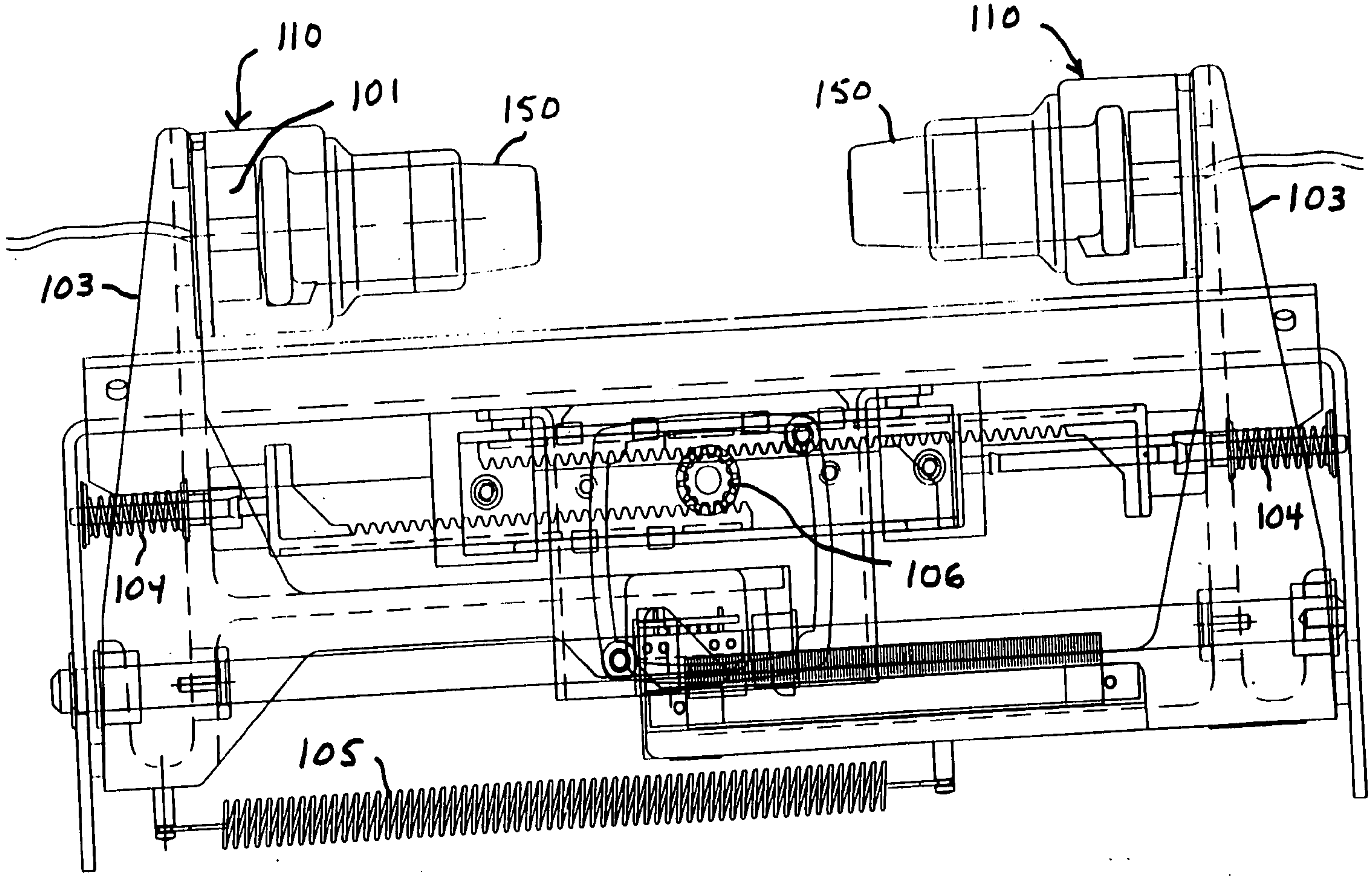


FIG. 3

FIG. 4A

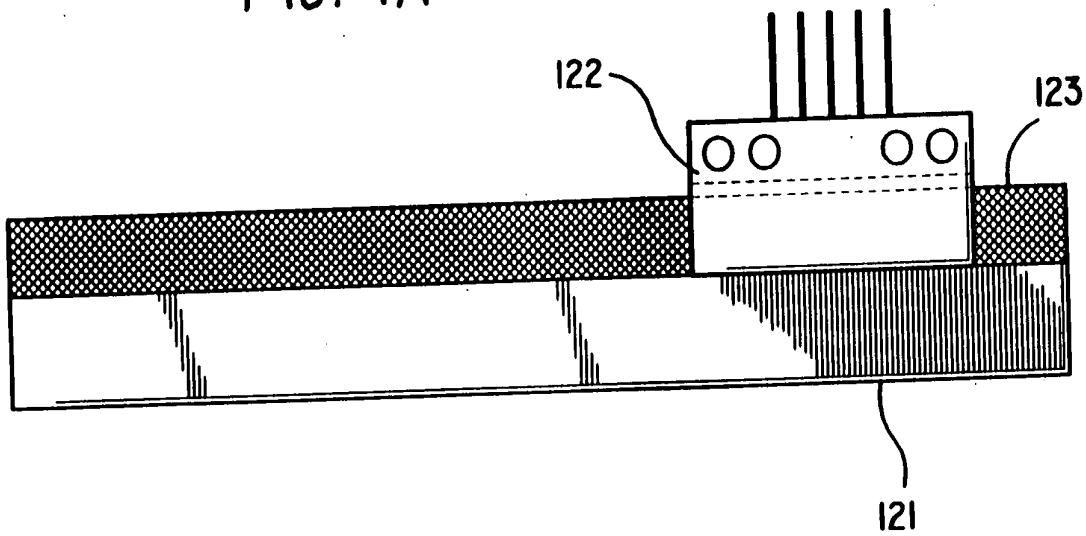


FIG. 4B

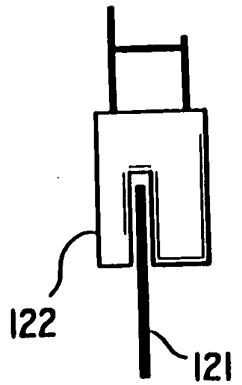
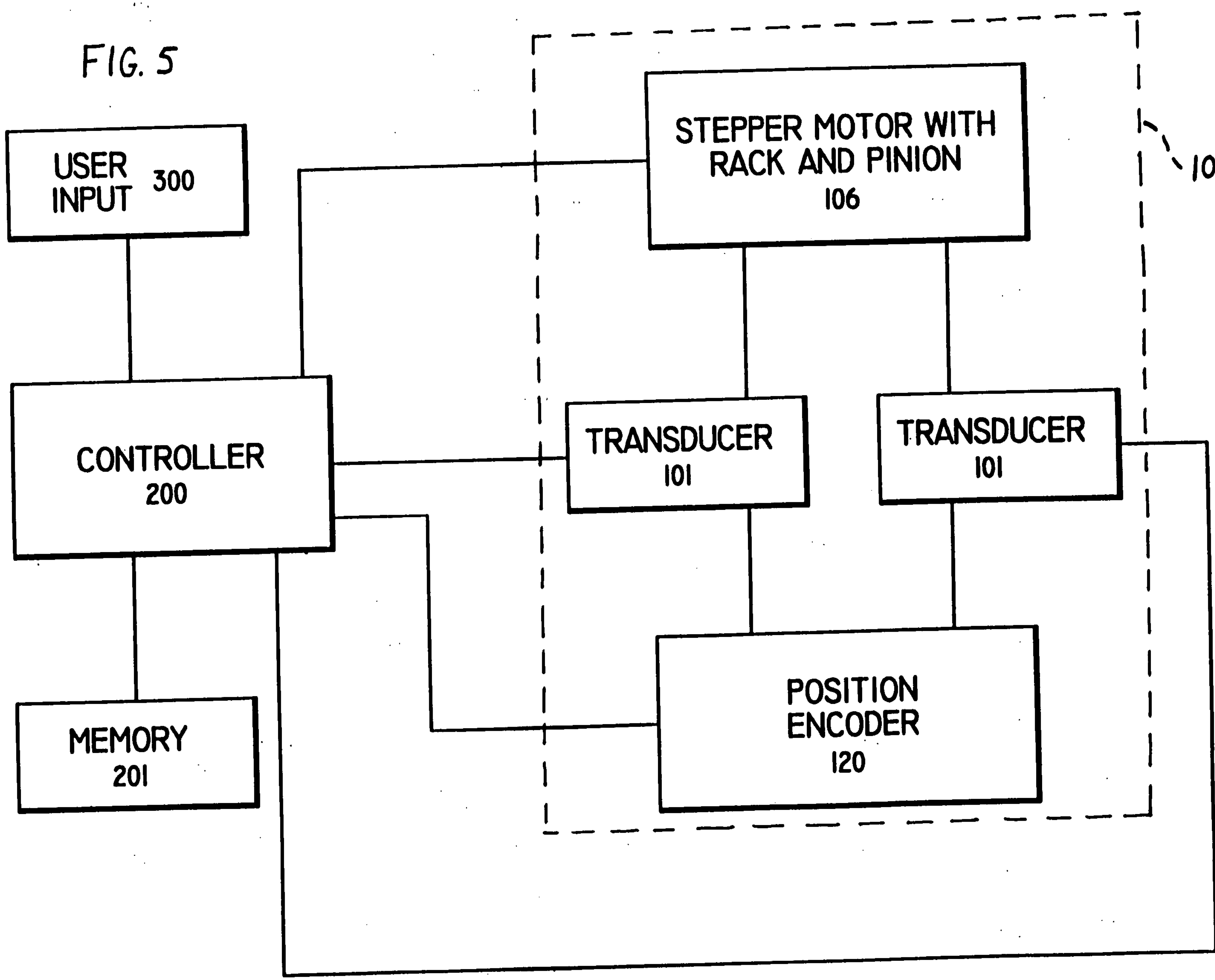


FIG. 5



USER INPUT 300
CONTROLLER 200
MEMORY 201
STEPPER MOTOR WITH RACK AND PINION 106
TRANSDUCER 101
TRANSDUCER 101
POSITION ENCODER 120
100

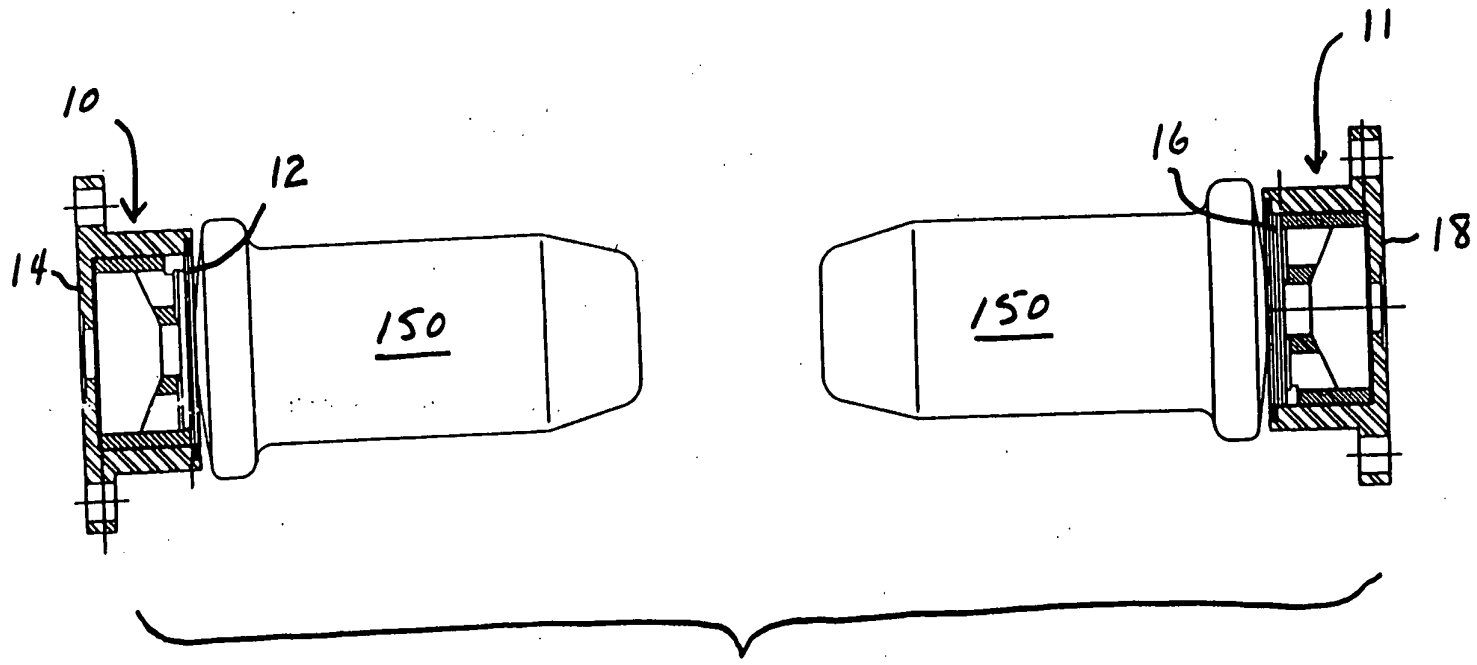


FIG. 6

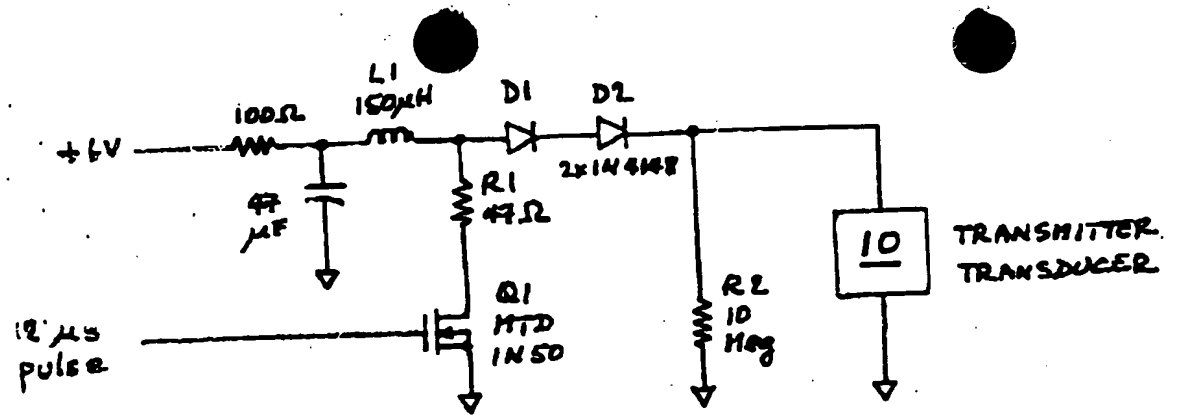

+6V
100Ω
L1
150μH
D1
D2
2x1N4148
47 μF
R1
47Ω
Q1
MTD
1N50
12 μs
pulse
R2
10
Meg
10
TRANSMITTER
TRANSDUCER

FIG. 7A

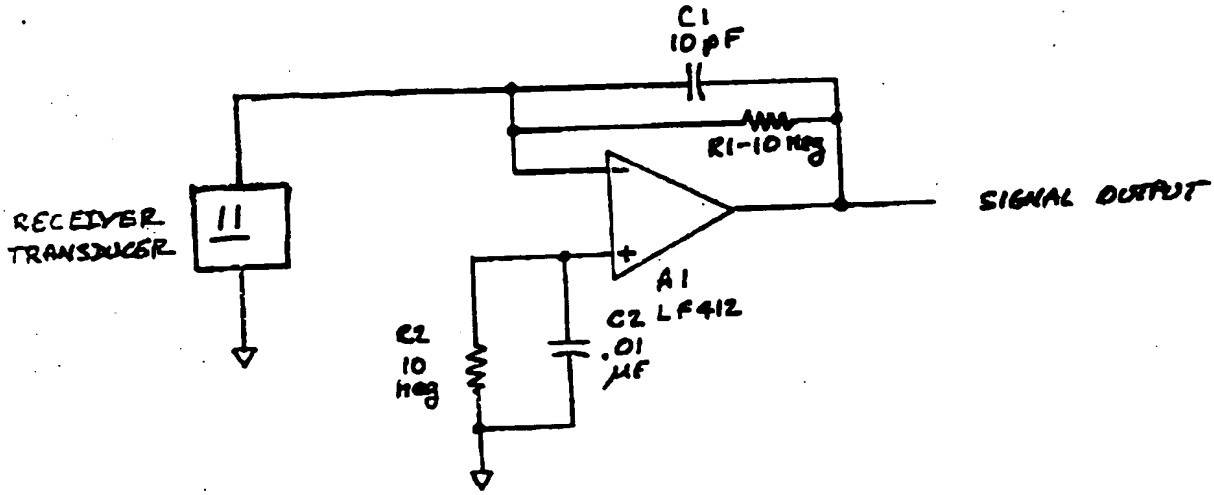

C1
10 pF
R1-10 Meg
RECEIVER
TRANSDUCER
11
SIGNAL OUTPUT
A1
LF412
C2
.01
μF
R2
10
Meg

FIG. 7B

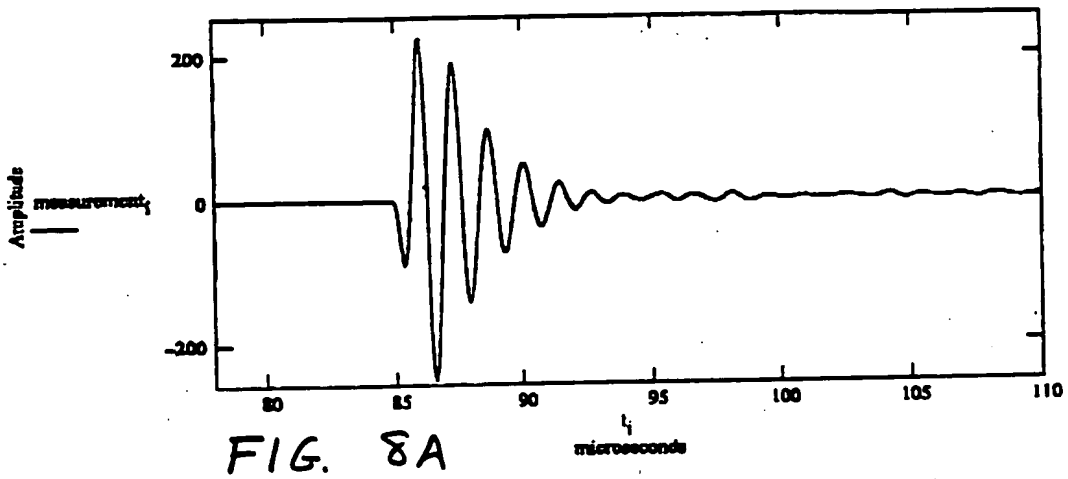


FIG. 8A

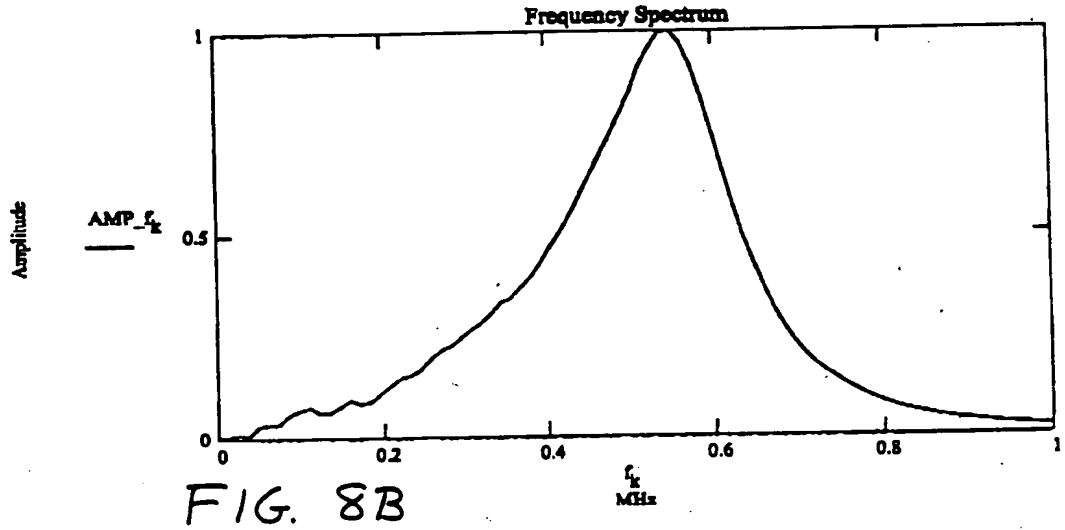


FIG. 8B

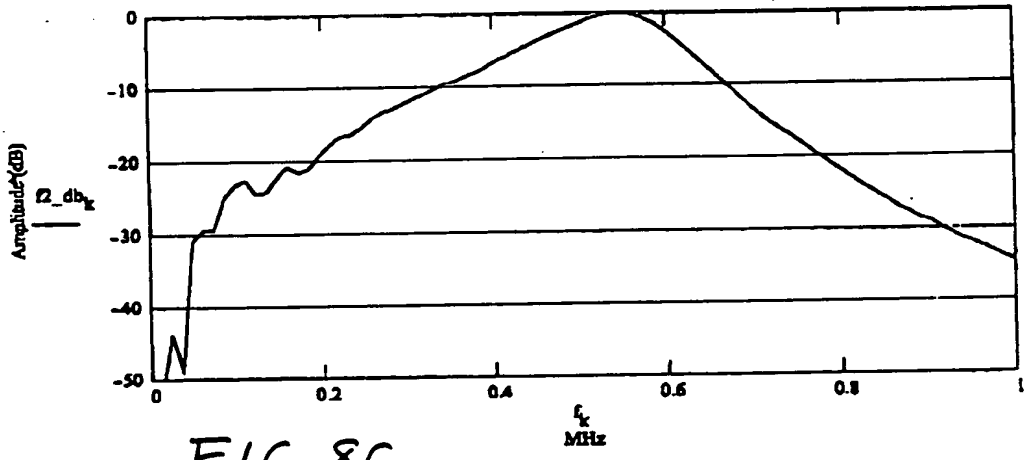


FIG. 8C

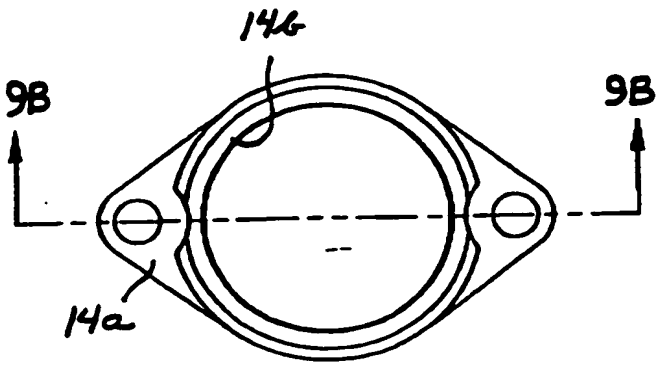


FIG. 9A

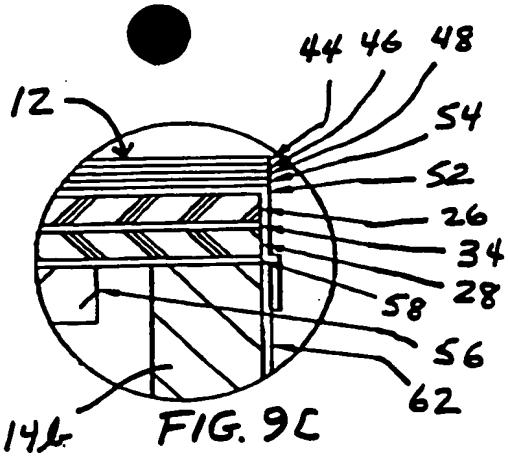


FIG. 9C

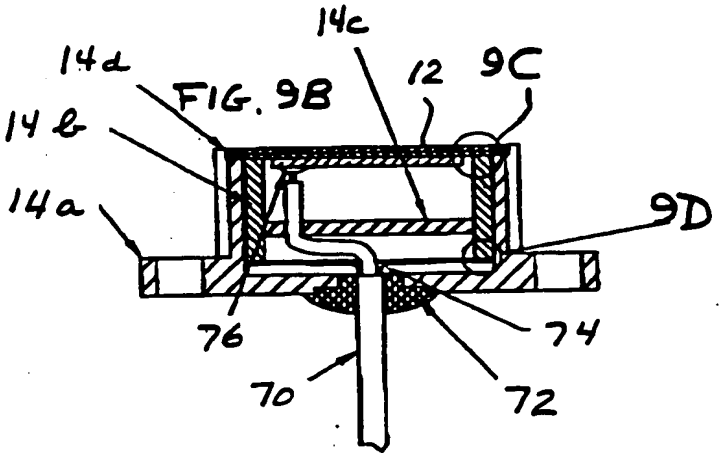


FIG. 9B

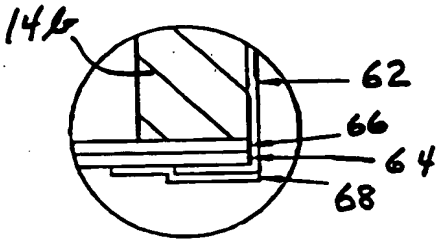


FIG. 9D

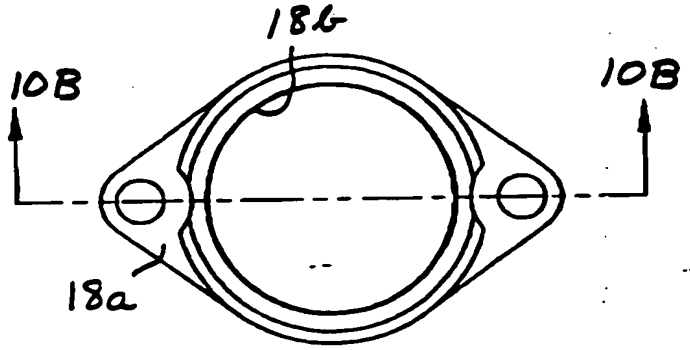


FIG. 10A

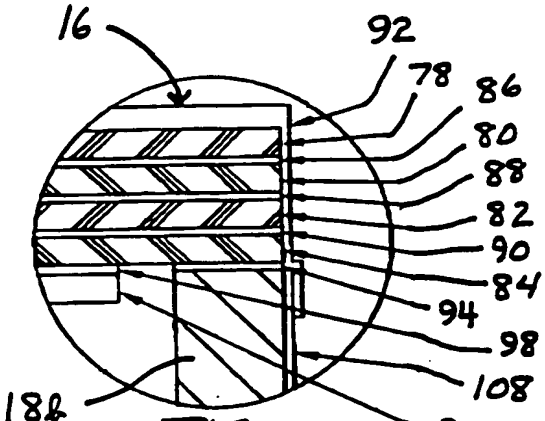


FIG. 10C

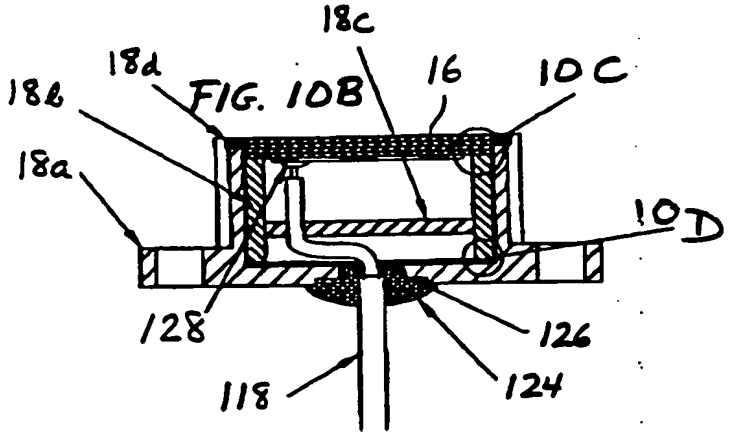


FIG. 10B

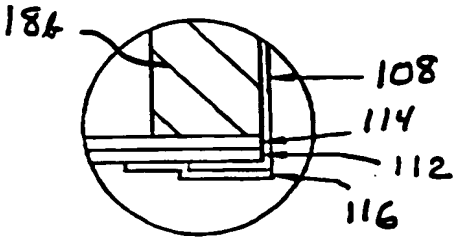
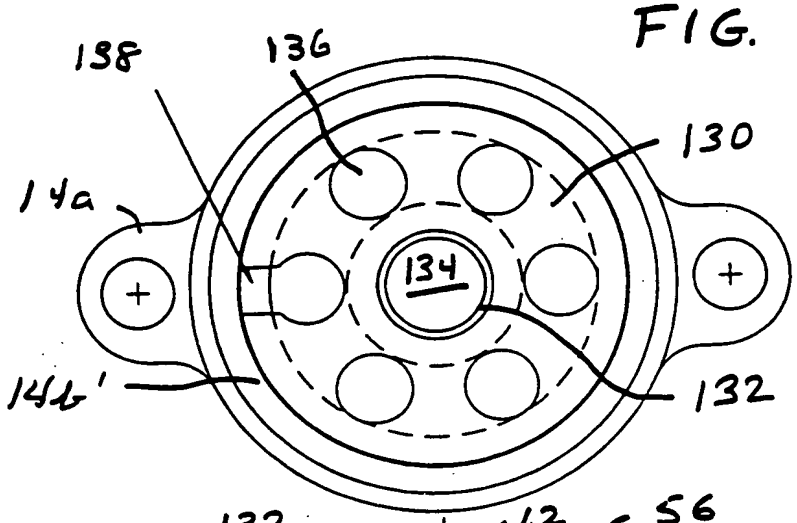


FIG. 10D

FIG. 13



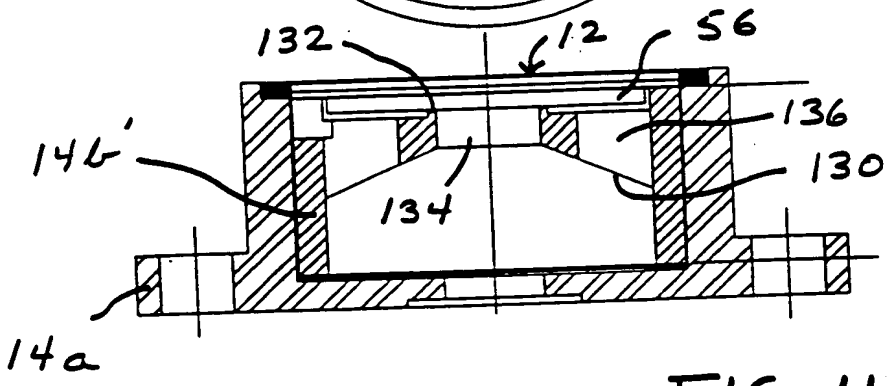


FIG. 11

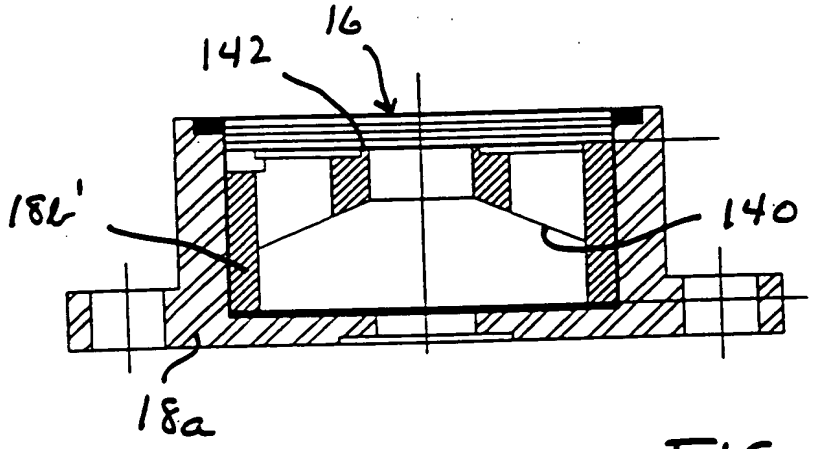


FIG. 12

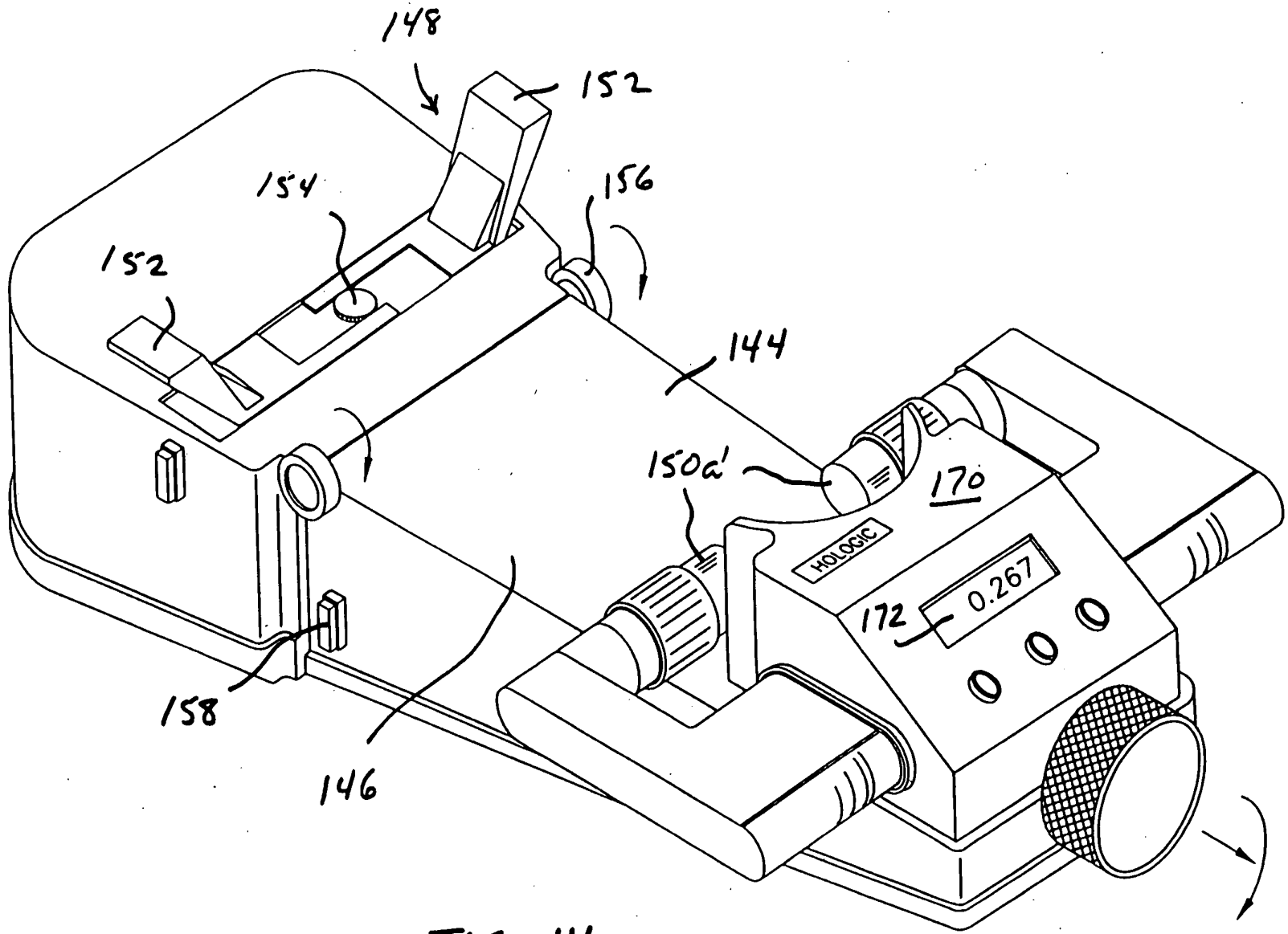


FIG. 14

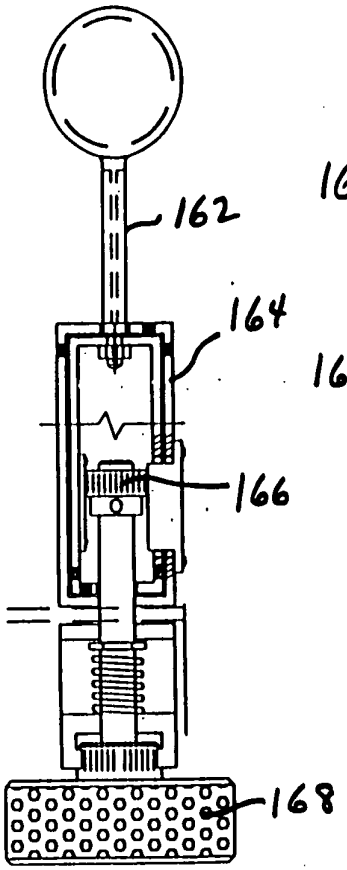


FIG. 15B

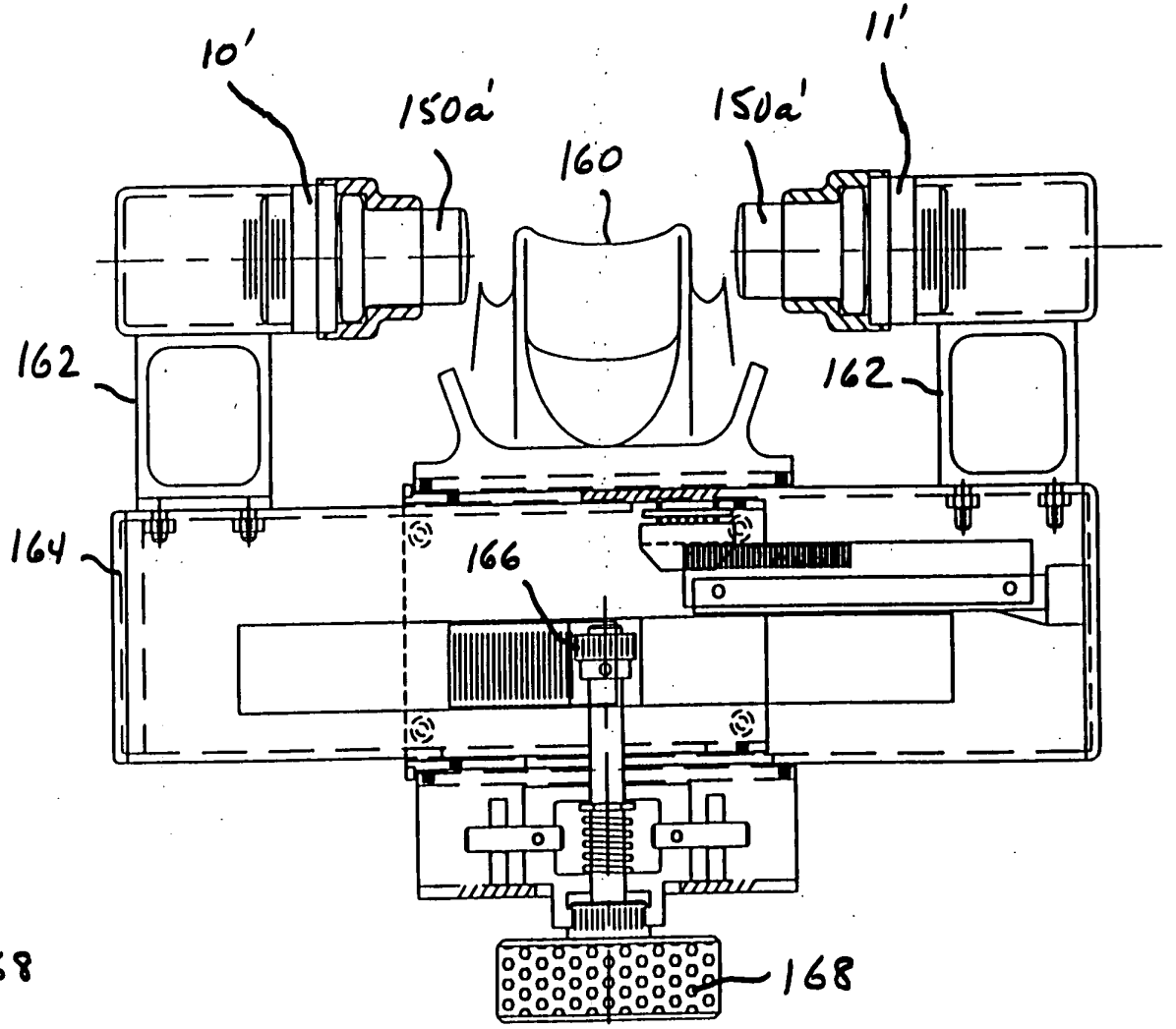


FIG. 15A

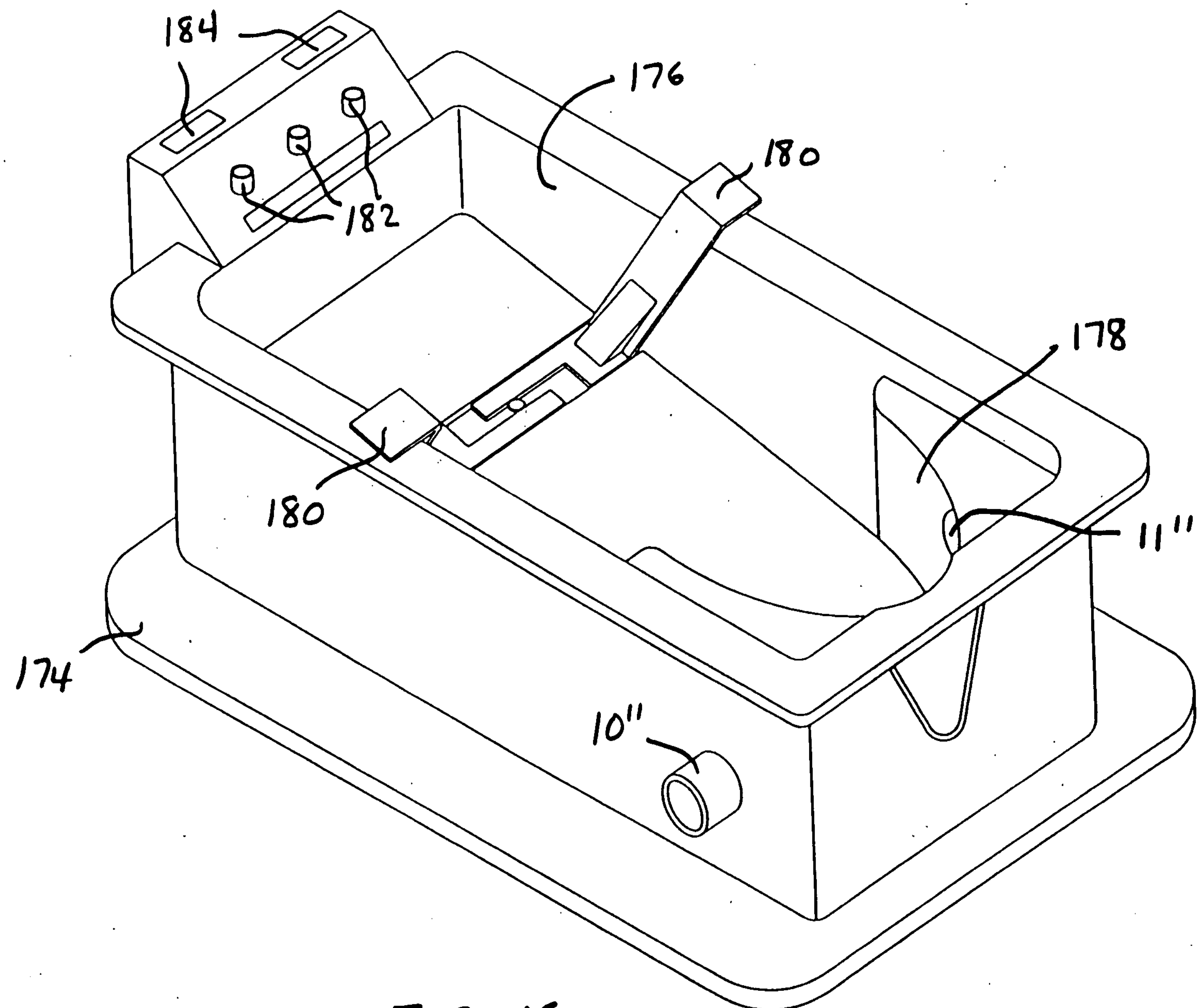


FIG. 16

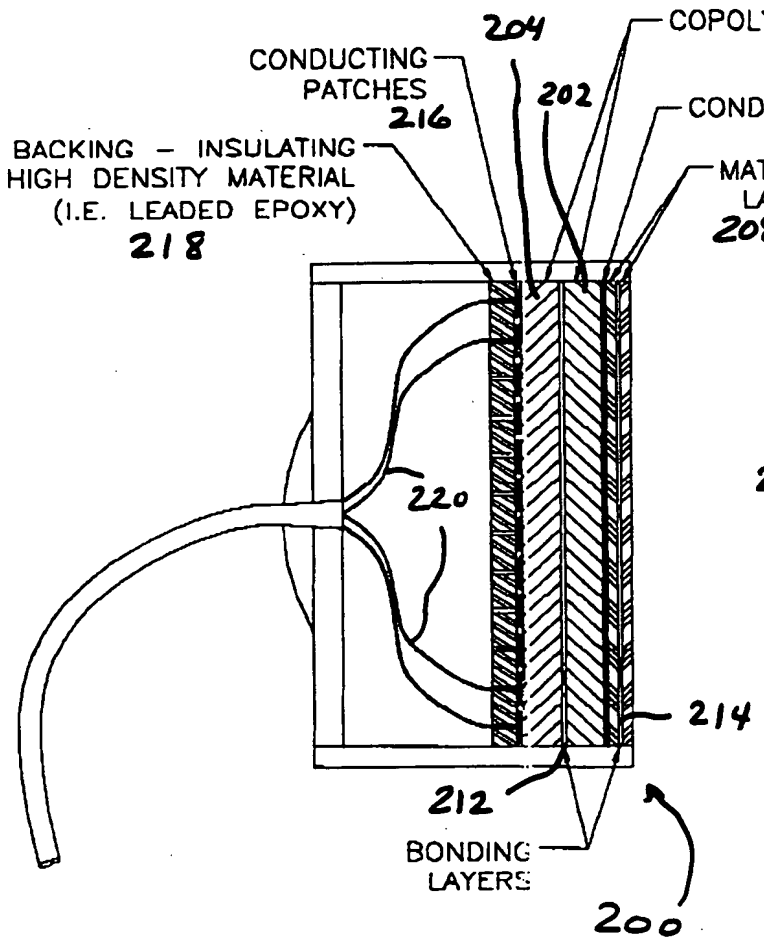


FIG. 17B

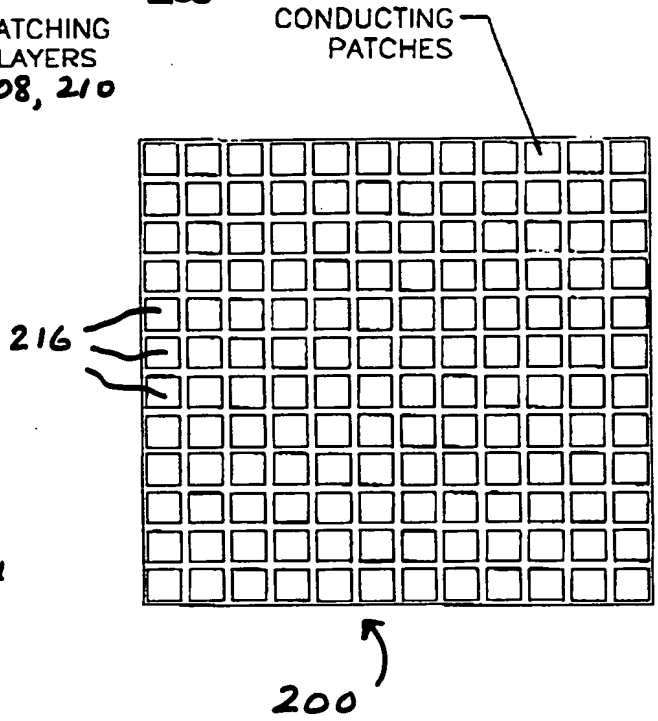


FIG. 17A

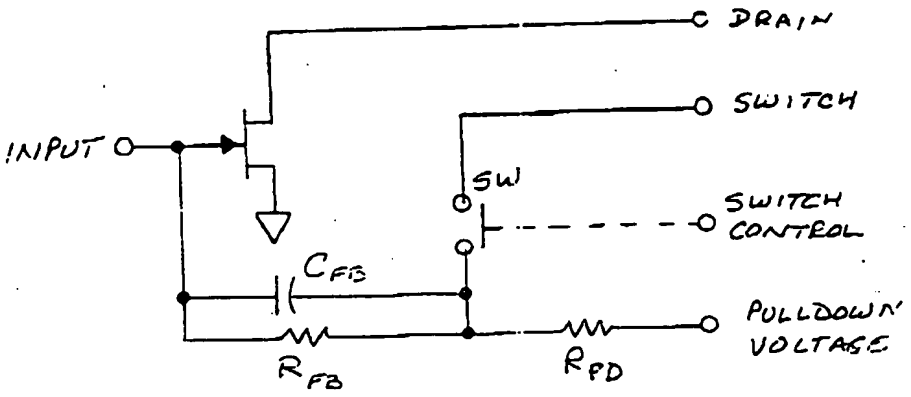


FIG. 18A N-Channel FET Input Stage

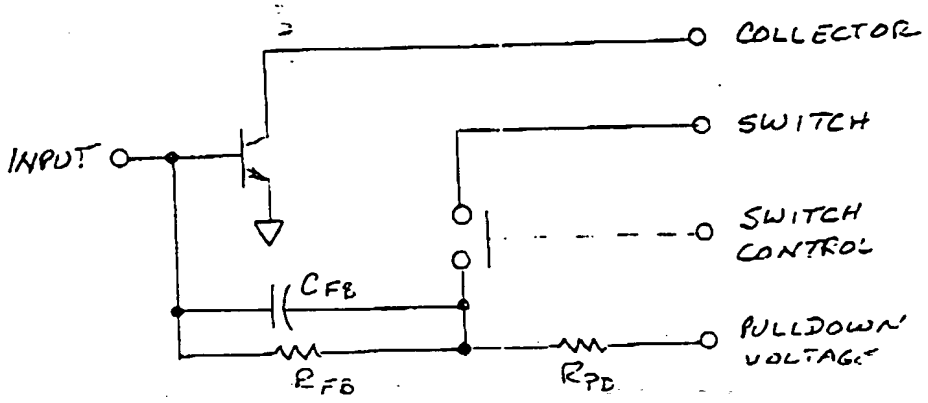


FIG 18B NPN Transistor Input Stage

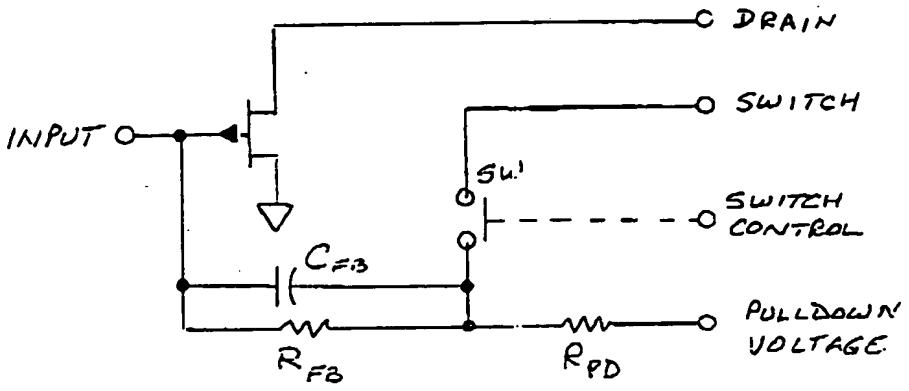


FIG. 18C – P-Channel FET Input Stage

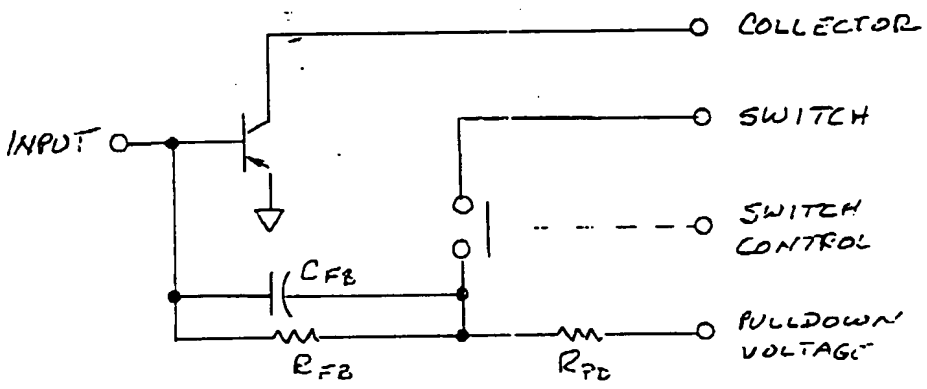


FIG 18D – PNP Transistor Input Stage

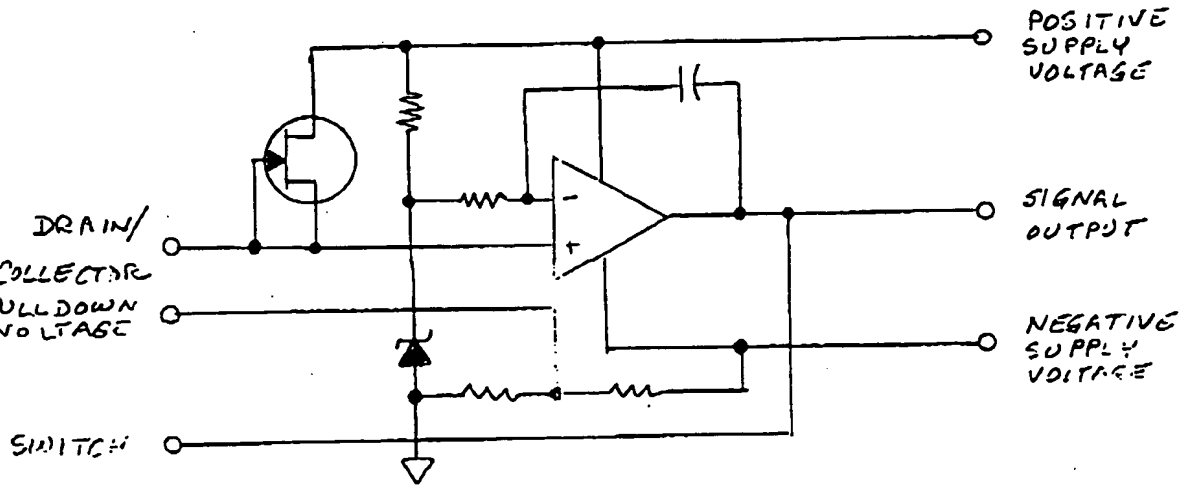


FIG 18E -- PREAMPLIFIER OUTPUT STAGE FOR N-CHANNEL OR NPN INPUT STAGE

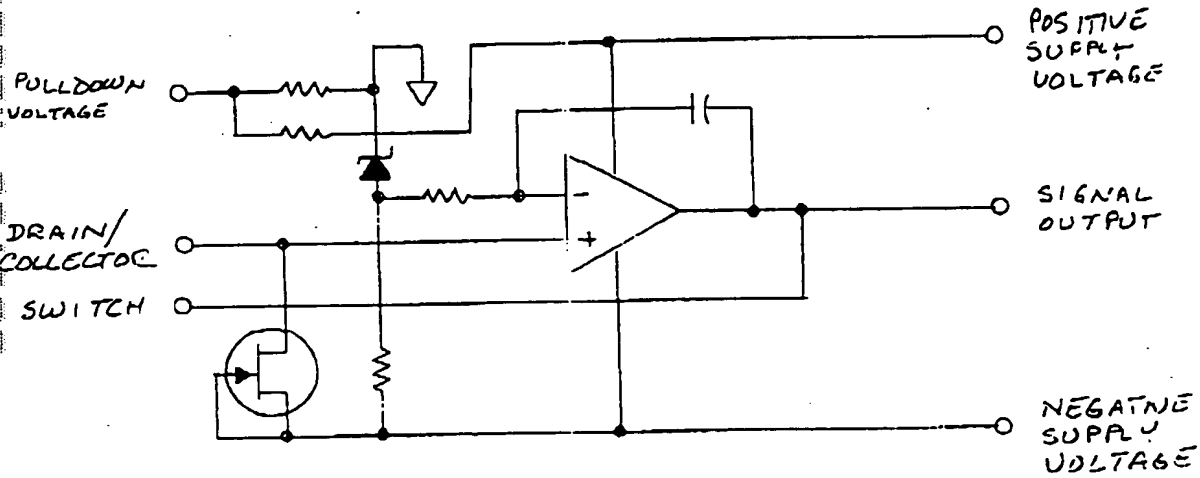


FIG. 18F -- PREAMPLIFIER OUTPUT STAGE FOR P-CHANNEL OR PNP INPUT STAGE